In the Claims:

1. (Currently Amended) A system comprising:

a first semiconductor device, and

a second semiconductor device,

wherein the first semiconductor device and the second semiconductor device each comprise a voltage supply device,

wherein said voltage supply device of said first semiconductor device is connected to said second semiconductor device, so that said voltage supply device of said first semiconductor device can provide a supply voltage for said second semiconductor device, and

wherein the system is adapted such that, in ~~a first~~ an external access operating mode of the second semiconductor device, the voltage supply device of said second semiconductor device provides the supply voltage for the second semiconductor device, and, in a ~~second~~ standby or refresh operating mode of the second semiconductor device, the voltage supply device of said first semiconductor device provides the supply voltage for the second semiconductor device.

2. (Previously Presented) The system according to claim 1, wherein said first semiconductor device and said second semiconductor device are arranged in a same housing.

3. (Previously Presented) The system according to claim 2, wherein said first and second semiconductor devices are arranged in said housing in a stacked manner.

4. (Previously Presented) The system according to claim 2, wherein said housing is a plug mountable semiconductor device housing.

5. (Previously Presented) The system according to claim 4, wherein said plug mountable semiconductor device housing is a Dual-In-Line (DIL) housing.

6. (Previously Presented) The system according to claim 4, wherein said plug mountable semiconductor device housing is a Pin-Grid-Array (PGA) housing.

7. (Previously Presented) The system according to claim 2, wherein said housing is a surface mountable semiconductor device housing.

8. (Previously Presented) The system according to claim 1, said system comprising one or several further semiconductor devices.

9. (Previously Presented) The system according to claim 8, wherein said one or said several further semiconductor device(s) is/are arranged in a same semiconductor device housing as said first and said second semiconductor devices.

10. (Previously Presented) The system according to claim 8, wherein said voltage supply device of said first semiconductor device is also connected to said one or to said several further semiconductor device(s), so that said voltage supply device of said first semiconductor device can additionally provide a supply voltage for said one or said several further semiconductor device(s).

11. (Previously Presented) The system according to claim 8, wherein said first semiconductor device comprises a further voltage supply device that is connected to said one or said several further semiconductor device(s), so that said further voltage supply device of said first semiconductor device can provide a supply voltage for said one or said several further semiconductor device(s).

12. (Previously Presented) The system according to claim 1, wherein said first and/or said second semiconductor devices, and/or said one and/or said several further semiconductor devices are memory devices.

13. (Previously Presented) The system according to claim 12, wherein said memory device is a table memory device or said memory devices are table memory devices, respectively.

14. (Previously Presented) The system according to claim 13, wherein said table memory device or said table memory devices are RAM table memory devices, respectively.

15. (Previously Presented) The system according to claim 14, wherein said RAM table memory device is a DRAM table memory device or said RAM table memory devices are DRAM table memory devices, respectively.

16. (Previously Presented) The system according to claim 13, wherein said table memory device is a ROM table memory device or said table memory devices are ROM table memory devices, respectively.

17. (Previously Presented) The system according to claim 12, wherein said memory device is or said memory devices are programmable logic devices (PLDs) and/or programmable logic arrays (PLAs).

18. (Previously Presented) The system according to claim 1, wherein said voltage supply device and/or said further voltage supply device provide a voltage supply for said first semiconductor device.

19. (Previously Presented) The system according to claim 1, wherein said voltage supply means and/or said further voltage supply means generate(s) the respective supply voltage from an external voltage.

20. (Previously Presented) The system according to claim 1, wherein said voltage supply device and/or said further voltage supply device are or comprise a voltage regulating device.

21. (Previously Presented) The system according to claim 1, wherein said voltage supply device and/or said further voltage supply device are or comprise a charge pump.

22. (Canceled)

23. (Previously Presented) The system according to claim 1, wherein said voltage supply device of said second semiconductor device is activated in the first operating mode, and wherein said supply voltage device of said second semiconductor device is deactivated in the second operating mode.

24. (Canceled).

25. (Canceled).

26. (Canceled).

27. (Previously Presented) The system according to claim 1, wherein an appropriate fuse is provided on said first and/or second semiconductor device(s), by means of which it is determined whether the corresponding semiconductor device is to assume the function of said first semiconductor device or the function of said second semiconductor device.

28. (Previously Presented) The system according to claim 1, wherein said voltage supply device of said first semiconductor device is connected to a corresponding pad of said first semiconductor device.

29. (Previously Presented) The system according to claim 28, wherein said pad of said first semiconductor device is connected to a pad which said voltage supply device of said second semiconductor device can be connected to.

30. (Previously Presented) The system according to claim 29, wherein said pad of said first semiconductor device is connected directly to the corresponding pad of said second semiconductor device by means of an appropriate bonding wire.

31. (Previously Presented) The system according to claim 29, wherein said pad of said first semiconductor device is connected indirectly to the corresponding pad of said second semiconductor device via an interposer.

32. (Previously Presented) The system according to claim 12, wherein said memory devices are functional memory devices.

33. (Previously Presented) The system according to claim 12, wherein said memory devices are fundamental memory devices.